

a substrate;
a P-well and an adjacent N-well formed in said substrate and defining a junction therebetween;
at least one P+ doped region dispersed in said N-well;
a N+ doped region dispersed in said P-well and coupled to ground;
at least one N+ doped trigger tap disposed proximate the at least one P+ doped region in said N-well; and
a PMOS transistor triggering device coupled to the SCR, wherein a drain is coupled to ground and a source is coupled to the trigger tap; the at least one P+ doped region is further coupled to a pad; the source is further coupled to the pad via a shunt resistor; and the pad is further coupled to said protected circuitry.

REMARKS

This Amendment is intended as a full and complete response to the non-final office action dated July 3, 2002. In the office action the Examiner notes that claims 1-31 are pending, of which claims 1-15 and 17-31 are rejected and claim 16 stands objected to. By this amendment, claims 2, 4, 15, 17, and 24 are amended and claims 3, 5-14, 16, 18-23, and 25-31 continue unamended.

In view of both the amendments presented above and the following discussion, the applicants submit that none of the claims now pending in the application are indefinite, anticipated or obvious under the respective provisions of 35 U.S.C. §112, §102 and §103. Thus, the applicants believe that all of these claims are now in allowable form.

It is to be understood that the applicants, by amending the claims, do not acquiesce to the Examiner's characterizations of the art of record or to applicants' subject matter recited in the pending claims. Further, applicants are not acquiescing to the Examiner's statements as to the applicability of the references of record to the pending claims by filing the instant responsive amendments.

A. IN THE DRAWINGS

The applicants have amended the Figures 1A, 1B, and 2A to conform the drawings to the specification. In particular, two reference designations 125 have been identified as signifying two different components. That is, reference number 125 was used to designate the substrate tie, as well as the drain of the triggering device. The applicants have amended the reference designation for the drain of the triggering device to new reference designation number 129.

Applicants have enclosed the proposed drawing corrections shown in red ink, and the applicants submit that such changed reference designation in Figs. 1A, 1B, and 2A do not add any new subject matter. Upon acceptance of these changes, the applicants will submit the formal drawings.

B. IN THE SPECIFICATION

The applicants have amended the specification to provide minor grammatical corrections and change the reference designations to conform to the reference designations in the drawings. Such grammatical corrections or reference designation changes do not add any new subject matter to the application.

C. ALLOWABLE SUBJECT MATTER

The Examiner has objected to claim 16 as being dependent upon a rejected base claim. The Examiner concludes that this claim would be allowable subject matter if rewritten in independent form including all the limitations of the base claim and any intervening claims.

The applicants thank the Examiner for indicating the allowable subject matter with respect to this claim. However, in view of the discussion set forth herein, the applicants believe that independent claim 15 is in allowable form and as such, dependent claim 16, as it stands, is also in allowable condition. Therefore, the applicants respectfully request that the foregoing objection to claim 16 be withdrawn.

D. REJECTIONS

(1) 35 U.S.C. §112

The Examiner has rejected claims 2, 4, 17, and 24-31 under 35 U.S.C. §112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. The applicants respectfully traverse this rejection.

(a) Claim 2

The applicants have amended claim 2 to change the limitation from "the lateral trigger device" to "the external trigger device". As such, the applicants submit that claim 2 is not indefinite and fully satisfies the requirements under 35 U.S.C. §112 and is patentable thereunder. Therefore, the applicants respectfully request that the rejection be withdrawn.

(b) Claims 4 and 17

The applicants have amended claims 4 and 17 to delete the limitation of "over a non high-doped region and". Therefore, clarification of the meaning of the limitation "a non high-doped region" is moot.

As such, the applicants submit that claims 4 and 17 are not indefinite and fully satisfy the requirements under 35 U.S.C. §112 and are patentable thereunder. Therefore, the applicants respectfully request that the rejections be withdrawn.

(c) Claim 24

The applicants have amended claim 24 to change the limitation of "at least one N+ doped trigger tap disposed proximate and between the at least one P+ doped region in said N-well" to "at least one N+ doped trigger tap disposed proximate the at least one P+ doped region in said N-well". Furthermore, the applicants have amended the limitations "the drain" and "the source" to "a drain" and "a source" to provide proper antecedent basis for these limitations.

As such, the applicants submit that claim 24 is not indefinite and fully satisfies the requirements under 35 U.S.C. §112 and is patentable thereunder. Furthermore, claims 25-31 depend, either directly or indirectly, from independent claim 24 and recite additional limitations thereof. As such, and for at least the same reasons as discussed above, the applicants submit that these dependent claims fully satisfy the requirements under 35 U.S.C. §112 and are patentable thereunder. Therefore, the applicants respectfully request that the rejection be withdrawn.

(2) 35 U.S.C. §102

The Examiner has rejected claims 1, 3-5, 7, 9, and 14 as being anticipated under 35 U.S.C. §102 by Polgreen, et al (U.S. Patent No. 5,465,189 issued November 7, 1995, hereinafter "Polgreen"). The applicants respectfully traverse the rejection.

The applicants' claim 1 recites:

"An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit having protected circuitry, the ESD protection circuit comprising:

a silicon controlled rectifier (SCR) having an anode coupled to the protected circuitry and a cathode coupled to ground, said cathode having at least one first high-doped region;

at least one trigger-tap, disposed proximate to the at least one high-doped region;

an external on-chip triggering device coupled to the trigger-tap and the protected circuitry." (emphasis added)

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim"

(Lindenmann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing Connell v. Sears Roebuck & Company, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). The Polgreen reference fails to teach each and every element of the claimed invention as arranged in the claim.

The Polgreen reference fails to teach or disclose "an external on-chip triggering device coupled to the trigger-tap and the protected circuitry." Rather, Polgreen discloses a MOS device that is integrated into the ESP protective circuitry and used as a SCR triggering device.

In particular, Polgreen discloses a lateral SCR wherein an NMOS device is integrated with the SCR device to provide triggering. Referring to figures 14, 16, and 18 of Polgreen, the NMOS trigger device is formed by the N+ cathode region in the P well, along with an N+ region disposed in both the P well and the N well. The gate 39 is formed over the P-well and between the two N+ regions to control the N channel. Moreover, the N+ cathode region also forms the emitter at the cathode of the SCR. Accordingly, the element that the Examiner refers to as the triggering device, is in fact, an element that is integrated with the SCR components, as opposed to being an external on-chip triggering device. By contrast, the applicants have provided a trigger device that is external to the SCR, which is coupled to the trigger tap and the protected circuitry. That is, components of the triggering device are not integrated (shared) with components of the SCR. Referring to figures 4 and 5 of the applicants' invention, it is clearly shown that the triggering device 205 is an on-chip device that is external to the SCR. Therefore, each and every element as arranged in the claim is not disclosed by the Polgreen reference.

As such, the applicants submit that independent claim 1 is not anticipated and fully satisfies the requirements under 35 U.S.C. §102 and is patentable thereunder. Furthermore, claims 3-5, 7, 9, and 14 depend, either directly or indirectly, from independent claim 1 and recite additional limitations thereof. As such, and for at least the same reasons as discussed above, the applicants submit that these dependent claims are not anticipated from the teachings of the reference and fully satisfy the requirements of 35 U.S.C. §102 and are patentable thereunder. Therefore, the applicants respectfully request that the rejections be withdrawn.

(3) 35 U.S.C. §103

(a) Claims 6 and 10-13

The Examiner has rejected claims 6 and 10-13 as being obvious under 35 U.S.C. §103 over Polgreen. The applicants respectfully traverse the rejection. Claims 6 and 10-13 depend either directly or indirectly from independent claim 1 and recite additional limitations thereof. In particular, claim 6 (and similarly claims 10-13) recites in part:

"An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit having protected circuitry, the ESD protection circuit comprising:

a silicon controlled rectifier (SCR) having an anode coupled to the protected circuitry and a cathode coupled to ground, said cathode having at least one first high-doped region;

at least one trigger-tap, disposed proximate to the at least one high-doped region;

an external on-chip triggering device coupled to the trigger-tap and the protected circuitry." (emphasis added)

The Polgreen reference fails to teach or suggest the applicants' invention as a whole. As discussed above, the Polgreen reference fails to teach or suggest "an external on-chip triggering device coupled to the trigger-tap and the protected circuitry." In fact, the Polgreen reference is completely devoid of any teaching or suggestion of an external on-chip triggering device. Rather, the Polgreen reference teaches away from the applicants' invention. Specifically, the Polgreen reference discloses an integrated triggering device coupled to the SCR and the protective circuitry. The structure of the lateral SCR device of the Polgreen reference and the problems associated with it was discussed in the background disclosure of the applicants' invention. In particular, the N+ region disposed between the P well and N well of Polgreen is equivalent to the drain region 110 in the prior art structure shown in figure 1B of applicants' invention. The N+ region 110 in applicants' invention and the N+ region in Polgreen is problematic when inserted as an integrated trigger means due to the excessive base widths of the NPN transistor and the PNP transistor of the SCR. The large lateral NPN and PNP transistor's dimensions due to the additional N+ diffusion region and the high recombination of charge carriers, results in slow SCR triggering. More specifically, by integrating that N+ region 110 of the triggering device into the SCR device, the current gain of the PNP transistor is reduced, which may impede or even prevent the SCR from triggering during an ESD event (see specification page 7, paragraph 20). Therefore, the Polgreen reference fails to teach or suggest the applicants' invention as a whole, since the Polgreen reference teaches away, as well as fails to embrace the problems in which the applicants' invention solves.

As such, the applicants submit that claims 6 and 10-13 are not obvious and fully satisfies the requirements under 35 U.S.C. §103 and are patentable thereunder. Therefore, the applicants respectfully request that the rejections be withdrawn.

(b) Claims 15, and 17-23

The Examiner has rejected claims 15, and 17-23 as being obvious under 35 U.S.C. §103 over Polgreen in view of the applicants' prior art (APA). The applicants respectfully traverse the rejection.

The applicants have amended independent claim 15 to recite limitations the applicants consider are inventive. In particular, claim 15 recites:

"An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit (IC) having protected circuitry, the ESD protection circuit comprising:
a SCR further comprising:
a substrate;
a N-well and an adjacent P-well formed in said substrate and defining a junction therebetween;
at least one N+ doped region in said P-well and coupled to ground;
a P+ doped region in said N-well and coupled to a pad of said protected circuitry;
at least one P+ doped trigger tap disposed proximate to at least one N+ doped region in said P-well; and
an external on-chip triggering device coupled to the SCR, wherein one terminal is coupled to the pad and a second terminal is coupled to the trigger tap." (emphasis added)

The combination of Polgreen and the applicants' prior art fails to teach or suggest the applicants' invention as a whole. In particular, the combined references fail to teach or suggest "an external on-chip triggering device coupled to the SCR, wherein one terminal is coupled to the path and a second terminal is coupled to the trigger-tap."

As discussed above, the Polgreen reference is completely devoid of any teaching or suggestion of an external on-chip triggering device. Rather, the triggering device in Polgreen is an integrated MOS device having an N+ doped region that forms the cathode of the SCR, as well as a drain region of the NMOS triggering device. Further, the applicants' admitted prior art fails to bridge a substantial gap as between the Polgreen reference and the applicants' invention. In particular, the APA discloses a similar structure as disclosed in the Polgreen reference. That is, the APA discloses an

N+ region 110 that forms the portion of the base of the PNP transistor, as well as the drain of the NMOS triggering device. Thus, Polgreen teaches that the NMOS triggering device is integrated with the SCR device. Even if these two references could possibly be combined (and the applicants submit that the two references may not be combined), neither reference, either singularly or in combination, teaches or suggests an external on-chip triggering device coupled to the SCR. Therefore, the combined references fail to teach or suggest the applicants' invention as a whole.

As such, the applicants submit that independent claim 15 is not obvious and fully satisfies the requirements under 35 U.S.C. §103 and is patentable thereunder. Furthermore, claims 17-23 depend, either directly or indirectly, from independent claim 15 and recite additional features thereof. As such, and for at least same reasons as discussed above, the applicants submit that these dependent claims are not obvious and fully satisfy the requirements under 35 U.S.C. §103 and are patentable thereunder. Therefore, the applicants respectfully request that the rejections be withdrawn.

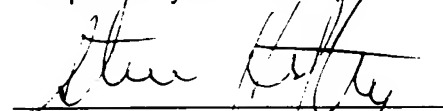
CONCLUSION

Thus, the applicants submit that none of the claims presently in the application are indefinite, anticipated or obvious under the respective provisions of 35 U.S.C. §112, §102 and §103. Consequently, the applicants believe that all these claims are presently in condition for allowance. Accordingly, reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Mr. Steven Hertzberg, telephone number (732) 530-9404, so that appropriate arrangements may be made for resolving such issues as expeditiously as possible.

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Respectfully submitted,


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